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MAFA: adaptive fault-tolerant routing algorithm for networks-on-chip, in: Proceeding of 15th Euromicro Conference on Digital System Design (DSD),

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Deadlock Free Routing Algorithm for Minimizing Data Packet Transmission in Network on Chip: 10.4018/jertcs.2012010104: Network on chip (NoC) has been proposed as a

Fault-aware and reconfigurable routing algorithms

IETE JOURNAL OF RESEARCH | VOL 57 | ISSUE 3 | MAY-JUN 2011 215 Fault-aware and Reconfigurable Routing Algorithms for Networks-on-Chip Mojtaba Valinataj, Siamak

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A Case for Bufferless Routing in On-Chip Networks Thomas Moscibroda Microsoft Research load-balanced adaptive routing algorithm for torus networks. In ISCA, 2003.

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Ville Rantala | Teijo Lehtonen | Juha Plosila Network on Chip Routing Algorithms TUCS Technical Report No 779, August 2006 Network on Chip Routing Algorithms Ville

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Designing Robust Routing Algorithms and Mapping Cores in Networks-on-Chip: A Multi-objective Evolutionary-based Approach. Maurizio Palesi (Kore University, Italy)

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viii Preface a brief introduction on the basic concepts of on-chip networks, routing algorithms for NoC architectures will be presented and discussed at different

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Chapter 5 Routing algorithms for workload consolidation Sophisticated routing algorithms can improve the network for adaptive routing in networks-on-chip.

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U. Saravanakumar, R. Rangarajan, R. Haripriya, R. Nithya and K. Rajasekar, "Cluster Based Hierarchical Routing Algorithm for Network on Chip," Circuits and Systems

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Provides a comprehensive overview of routing algorithms for Networks-on-Chip and NoC-based, manycore systems ; Describes routing algorithms for NoC architectures at

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