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IETE JOURNAL OF RESEARCH | VOL 57 | ISSUE 3 | MAY-JUN 2011 215 Fault-aware and Reconfigurable Routing Algorithms for Networks-on-Chip Mojtaba Valinataj, Siamak

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Ville Rantala | Teijo Lehtonen | Juha Plosila Network on Chip Routing Algorithms TUCS Technical Report No 779, August 2006 Network on Chip Routing Algorithms Ville

Application specific routing algorithms for

In this paper, we present a methodology to design highly adaptive routing algorithms for NoC architectures that do not require the use of any VCs.

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Network on chip or network the algorithms must be designed in such a way that they offer large parallelism The routing algorithms should be implemented

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viii Preface a brief introduction on the basic concepts of on-chip networks, routing algorithms for NoC architectures will be presented and discussed at different

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A Case for Bufferless Routing in On-Chip Networks Thomas Moscibroda Microsoft Research load-balanced adaptive routing algorithm for torus networks. In ISCA, 2003.

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MAFA: adaptive fault-tolerant routing algorithm for networks-on-chip, in: Proceeding of 15th Euromicro Conference on Digital System Design (DSD),

Cluster based hierarchical routing algorithm for

U. Saravanakumar, R. Rangarajan, R. Haripriya, R. Nithya and K. Rajasekar, "Cluster Based Hierarchical Routing Algorithm for Network on Chip," Circuits and Systems

Deadlock free routing algorithm for minimizing

Deadlock Free Routing Algorithm for Minimizing Data Packet Transmission in Network on Chip: 10.4018/jertcs.2012010104: Network on chip (NoC) has been proposed as a

Designing robust routing algorithms and mapping

Designing Robust Routing Algorithms and Mapping Cores in Networks-on-Chip: A Multi-objective Evolutionary-based Approach. Maurizio Palesi (Kore University, Italy)

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